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05SCS11/05SCE11

First Semester M.Tech Degree Examination, Dec. 07 / Jan. 08
Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain the operations of Flynn's classification of computer architecture. **(10 Marks)**

b. Distinguish between multiprocessors and multi-computers based on their structures, resources sharing and interprocessor communications. **(10 Marks)**

2 a. Discuss the various dependencies that can cause problems to the smooth flow of instructions through pipelines, with examples. **(10 Marks)**

b. What is instruction scheduling? Discuss the different ILP – instruction scheduling schemes. **(10 Marks)**

3 a. What is the role of rename registers in super scalar processing? Explain with an example. **(10 Marks)**

b. Explain the importance of preserving sequential consistency in superscalar processors. **(10 Marks)**

4 a. Explain the BTAC and BTIC branch target accessing schemes. In what way they differ? **(10 Marks)**

b. What is shelving? Explain the principle of shelving in superscalar processors. **(10 Marks)**

5 a. A certain dynamic pipeline with 4 stages is characterized by the following reservation table:

	time						
	t_0	t_1	t_2	t_3	t_4	t_5	t_6
S1	X					X	
S2			X				X
S3		X		X			
S4			X		X		

Stages

Obtain the collision vector, state transition diagram, forbidden latencies, simple cycles, greedy cycles and MAL. **(10 Marks)**

b. Distinguish between linear pipelining and non-linear pipelining. Derive the expressions for speedup, efficiency and throughput for linear pipelines. **(10 Marks)**

6 a. With a block diagram, explain a pipeline unit for fixed-point multiplication of 8-bit integers. **(10 Marks)**

b. Write a block diagram and explain with an example the operation of a data flow computers. **(10 Marks)**

7 a. Draw a 8×8 Omega network using 2×2 switches. From your network, show the following simultaneous connections between input and output:

i/p : 0 4 3 6 7 5 2 1

o/p : 6 7 0 4 3 1 2 5

Is the network blocked? If it is blocked, how can you resolve the conflict? **(10 Marks)**

b. Explain the systolic architecture for matrix multiplication. **(10 Marks)**

8 a. How bus snooping can be used to avoid the cache coherence? What are the demerits of this strategy? **(10 Marks)**

b. Write short notes on: i) VLIW architecture ii) Architecture of Power PC 620. **(10 Marks)**

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